NHR FAU

FAU Friedrich-Alexander-Universität Erlangen-Nürnberg

# Programming Techniques for Supercomputers Tutorial

Erlangen National High Performance Computing Center

Department of Computer Science

FAU Erlangen-Nürnberg

Sommersemester 2026

# Assignment 2 – Task 1 a)

## Peak Performance

- Clock frequency of 2.05 GHz, but only 0.9 * 2.05 GHz for “hot code”
- 126 cores
- ShmAVX-1024 instruction set (1024-bit wide SIMD registers); each core is capable of retiring one full-width double-precision FMA instruction per cycle

$$P_{peak} = n_{cores} * n_{super}^{FP} * n_{FMA} * n_{SIMD} * f$$

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When in doubt, think **units**!

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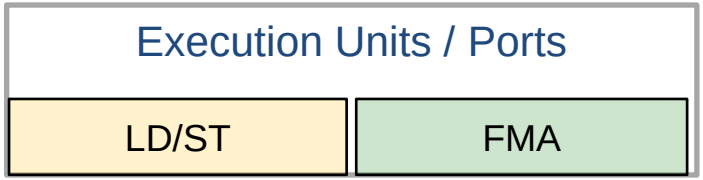
# Assignment 2 – Task 1 b)

## Execution Units

```
double a[...],b[...];
double s=0.0, t=1.234;
// a[] and b[] contain sensible data
for(int i=0; i<N; ++i) {
  s += a[i]*a[i];
  b[i] *= t;
}
```




- Capability of executing 1 FMA, and 1 LOAD or 1 STORE instruction per cycle
- 1024-bit wide SIMD capability, for all instructions

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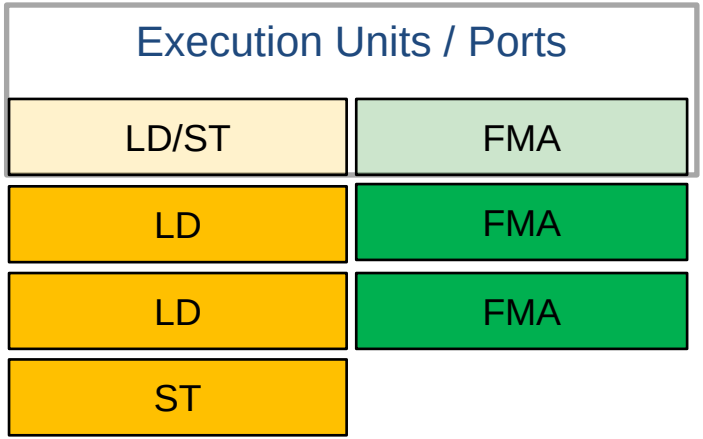


- Suppose the MULT uses the FMA port and adds “zero”
- Two FMAs, 2 LOAD, and 1 STORE

$$P_{\max} = 126 * \frac{1[iter]}{3[cy]} * 1.845 \left[\frac{Gcy}{s}\right] = 126 * \frac{3*16[flops]}{3[cy]} * 1.845 \left[\frac{Gcy}{s}\right] = 3.720 \left[\frac{Gflops}{s}\right]$$

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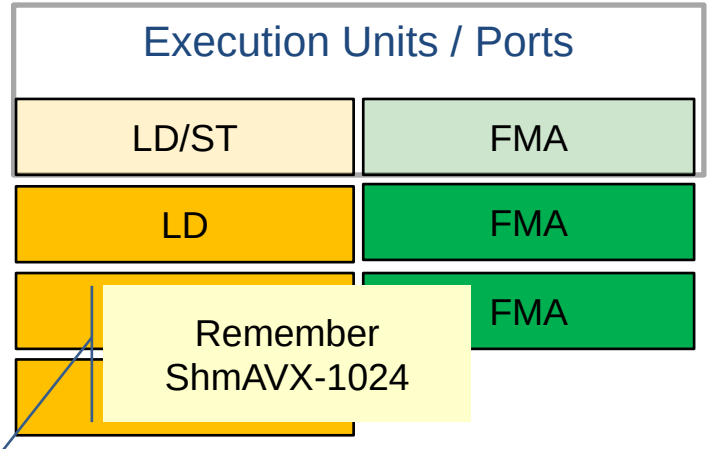


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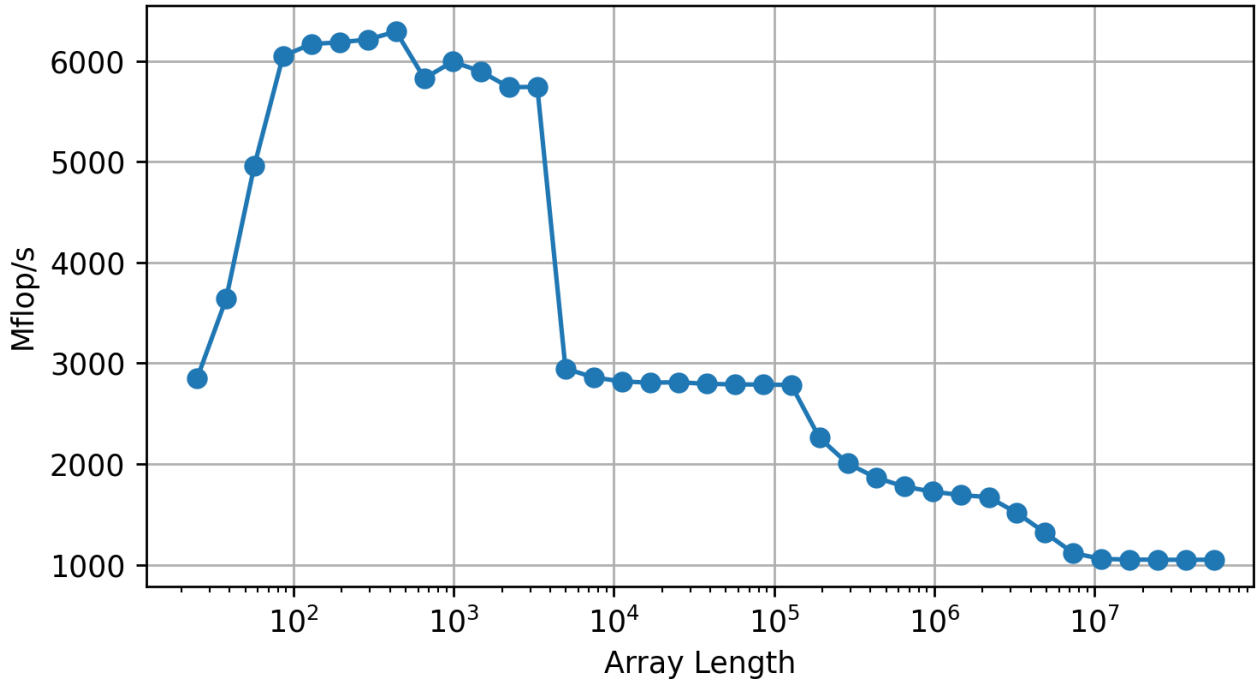
## Loop Kernel Benchmarking

a) Accumulate: `a[i] = a[i] + b[i]`

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L2 cache: 1.25 MiB
L3 cache: 54 MiB

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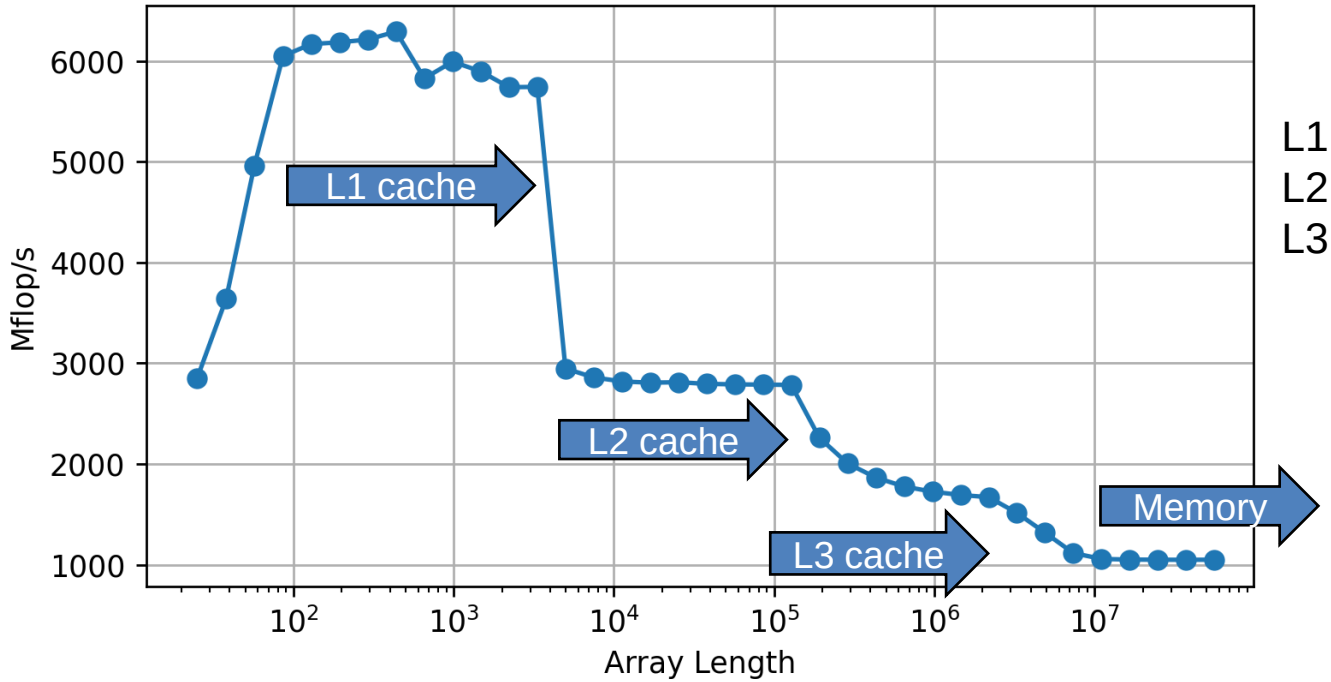


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## Loop Kernel Benchmarking

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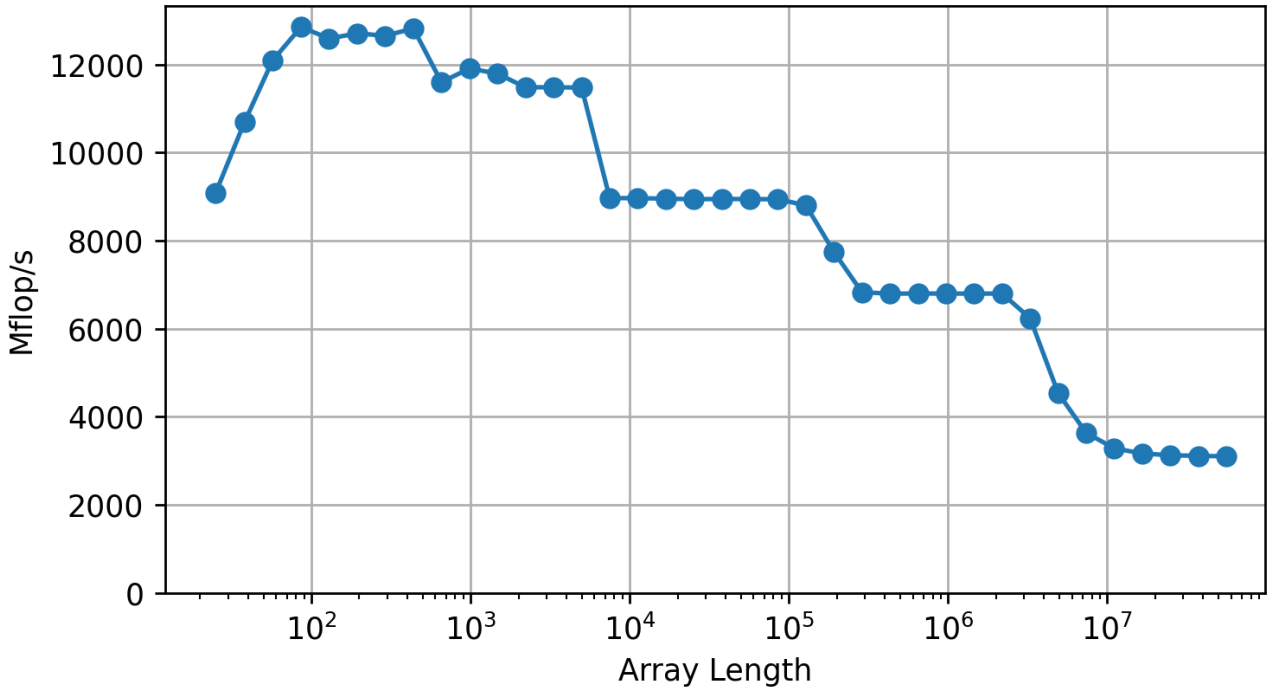


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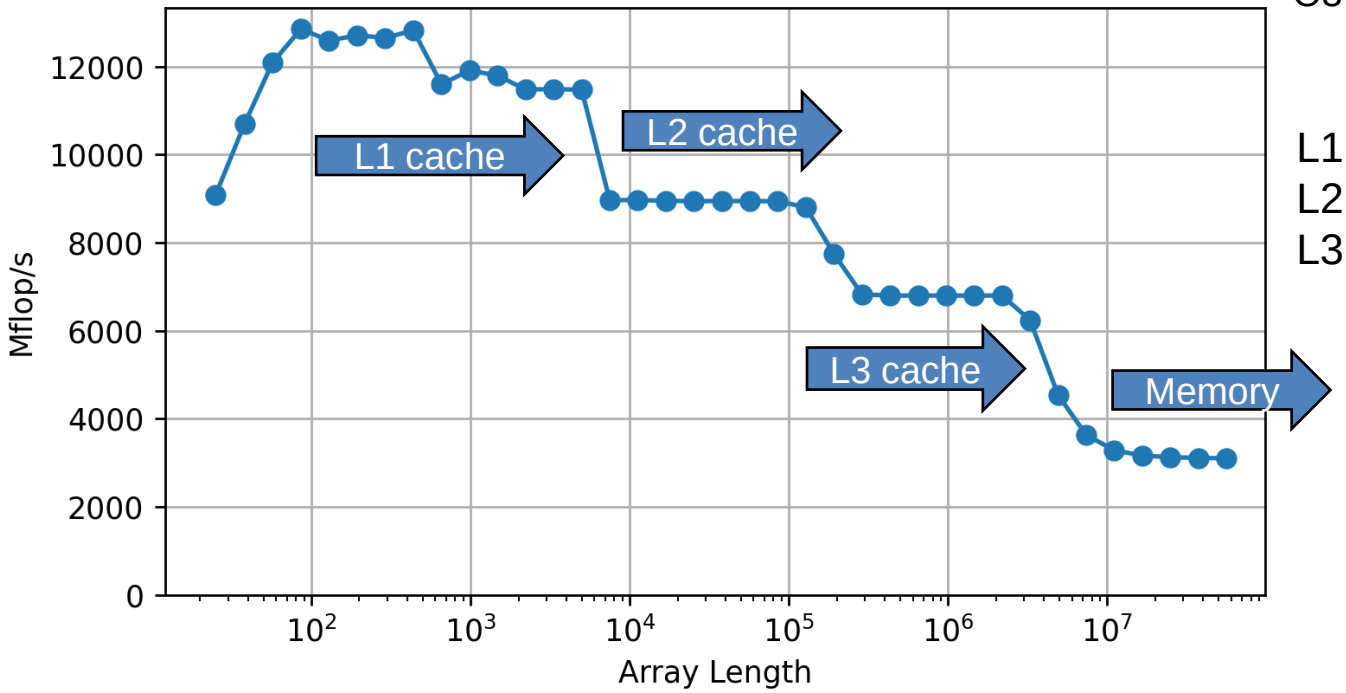


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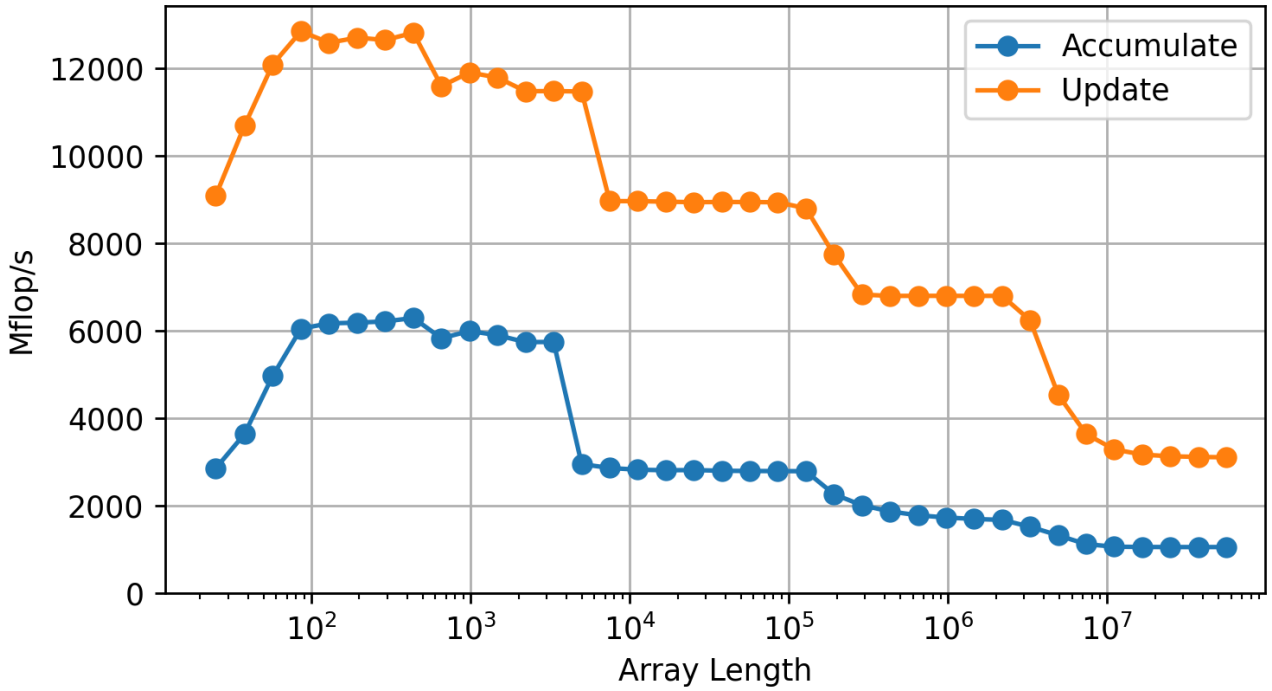
## Loop Kernel Benchmarking

d) Differences

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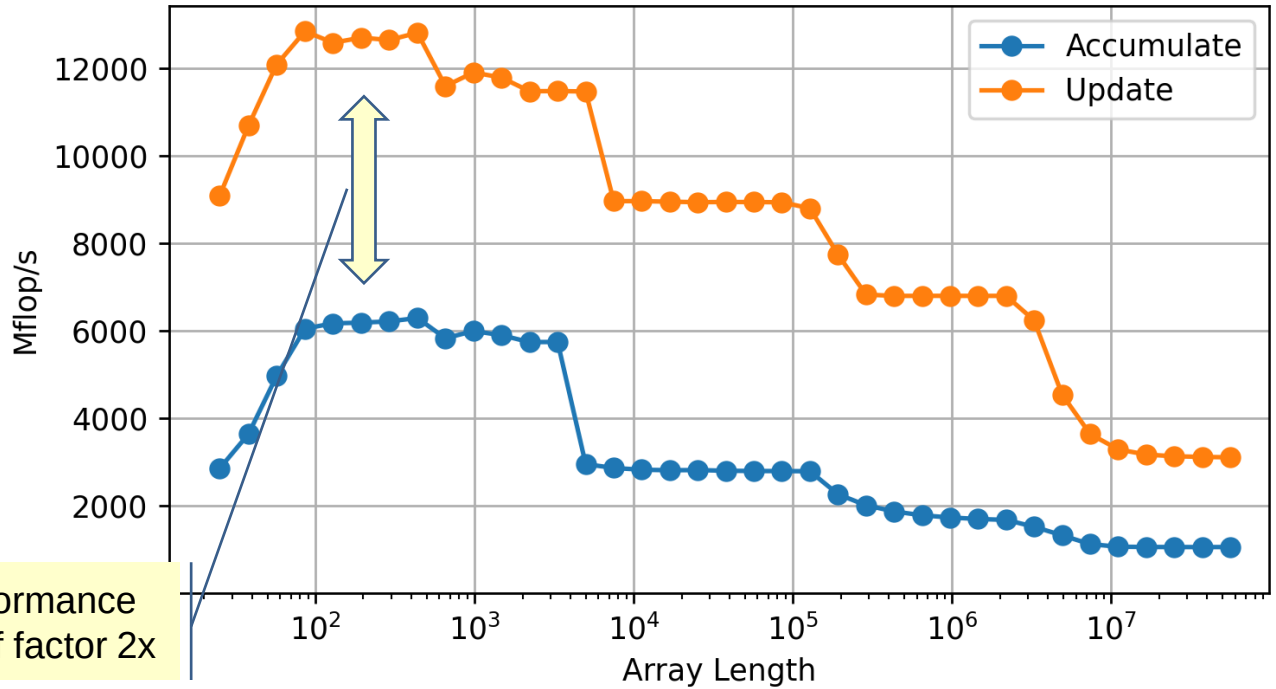


Performance diff. of factor 2x

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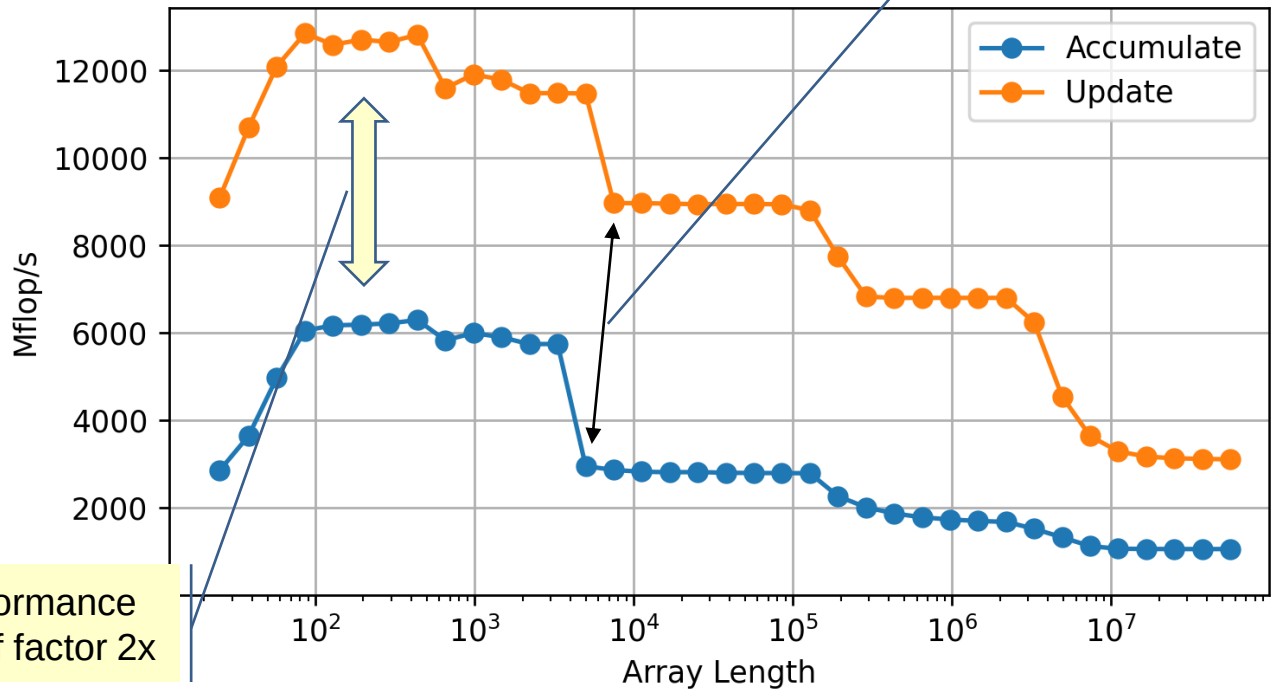
## Loop Kernel Benchmarking

d) Differences




Drops appear 2x later. Why?

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